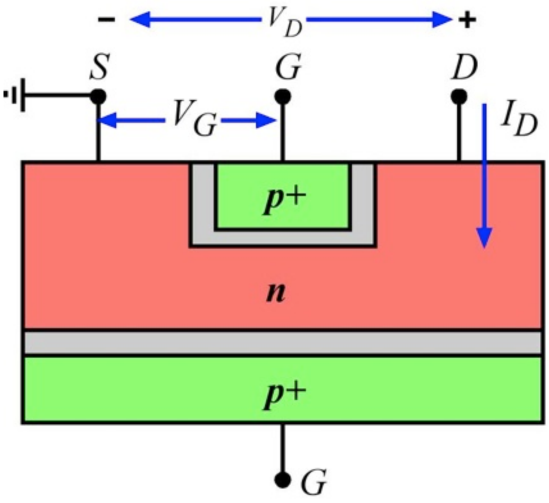
EECS 2077
Semiconductor
Devices

11 - JFET MESFET HEMT

Name:______________________________ Complete ____

Agenda: (1) review the quiz / (2) 5 minutes minimum for lecture questions and review / (3) start the problems!

In-Class Problems



(1) Let's design a JFET. An ideal Si p+n junction at 300K has the following parameters (you may or may not need them all).

p-side:	n-side:	General parameters
$Na=10^{17}/cm^3$	$Nd=10^{15}/cm^3$	$A=10^{-6}$ cm^2
$Dn=18$ cm^2/sec	$Dp=25$ cm^2/sec	$\varepsilon_{Si}=11.8$
$Ln=10^{-3}$ cm	$Lp=10^{-2}$ cm	
μp=200 cm2/V-s	μn=1300 cm2/V-s	
μn=700 cm2/V-s	μp=450 cm2/V-s	

$V_o=0.0259*\ln(10^{32}/2.25\times10^{20})=0.695V$

a) Calculate the drift current across the junction at no applied bias (0V). This will be the amount of JFET gate current you need. Is it small or large?

$$I_o \simeq qA\left(\frac{D_p}{L_p}p_n\right) = 1.6\times10^{-19}\cdot10^{-6}\cdot\left(\frac{25}{10^{-2}}\right)\cdot2.25\times10^{5} = 9\times10^{-17}A$$

$$p_n = \frac{n_i^2}{N_D} = \frac{(1.5\times10^{10})^2}{(10^{15})} = 2.25\times10^{5}/cc$$

Note, for a JFET, this are TWO junctions so the total gate current would be double.

b) Calculate the width of the depletion region (W) at no applied bias (0V).

$$W = \left[\frac{2\varepsilon_r\varepsilon_o V_o}{q}\left(\frac{1}{N_D}\right)\right]^{1/2} = \left[\frac{2\cdot11.8\cdot8.854\times10^{-14}\cdot0.695}{1.6\times10^{-19}\cdot10^{15}}\right]^{1/2}$$

$$= 9.5\times10^{-5}cm = 0.95\,\mu m$$

c) You use the above materials to make a JFET. If you want a conducting portion of the channel that is at least 3 μm thick, what is the distance you will need between the semiconductor regions making up the gate?

> Each depletion region will be 0.95 μm into the n-type semiconductor mainly, so at least >1.9 μm distance to have any channel at all, + 3 μm = 4.9 μm total. For the next part you will need a=4.9 μm / 2 or a=2.45 μm.

d) How much gate voltage then will it require to turn this JFET fully OFF?

If W at 0V is 0.95 μm, then to turn this JFET off you will need another 1.5 μm from each junction (W=2.45 μm).

V+Vo = (2.45E-4)^2 / 2 / 11.8 / 8.854 E-14 /*1.6E-19*1E15 = 4.59 V.

V= 4.59 – 0.695 = 3.9 V

e) Lastly, calculate the maximum output current for the case where the source is grounded (0V). Assume that the length of the channel (L) is 3.16 µm and the depth (Z) of the channel is 31.6 µm (ends up being like the area we listed above at 1E-6 cm^2, Z/L = 10). You will need ‘a’ too, but that is easy as you can get it from part (c).

Since you know what was the source voltage is, then you should be able to easily see what you should have for Vg, and then plug away at the equation below. Compare this to the amount of current required to reverse bias the gates and comment.

$$I_D(sat.) = G_0 V_P \left[\frac{V_G}{V_P} - \frac{2}{3}\left(\frac{V_G}{V_P}\right)^{3/2} + \frac{1}{3} \right] \qquad V_p = \frac{q a^2 N_D}{2\varepsilon} \qquad G_0 = \frac{2aZ}{\rho L} \qquad \sigma = q\mu_n n_0 = \rho^{-1}$$

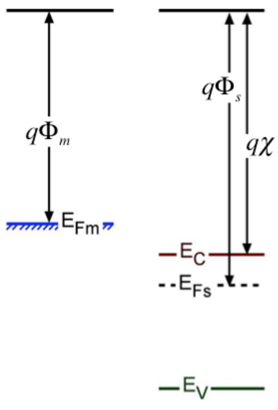
Vg = 0V (we want min depletion, but we also can’t forward biase the gate-source region, so must be 0V)

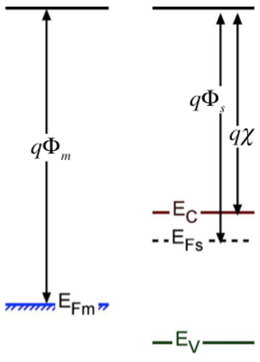
Rho = 1/(1.6E-19*1300*1E15) = 4.81 ohm-cm

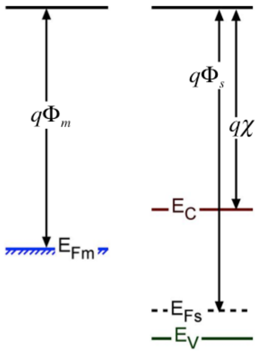
Vp =1.6E-19*2.45^2*1E15/2/ (8.8.54E14*11.8) = 4.6 V

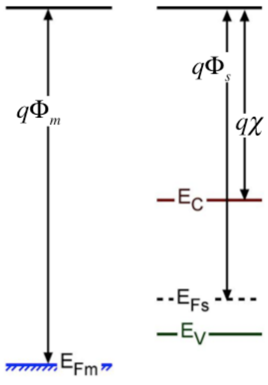
Id = 2 * 2.45E-4 / 4.81 * 10 * 4.6 / 3 = 1.6 mA!

(2) Which of the following metal-semiconductor contacts can be used to construct a MESFET gate? Just <u>quickly</u> and roughly sketch the band diagrams to see if they are ohmic or rectifying.



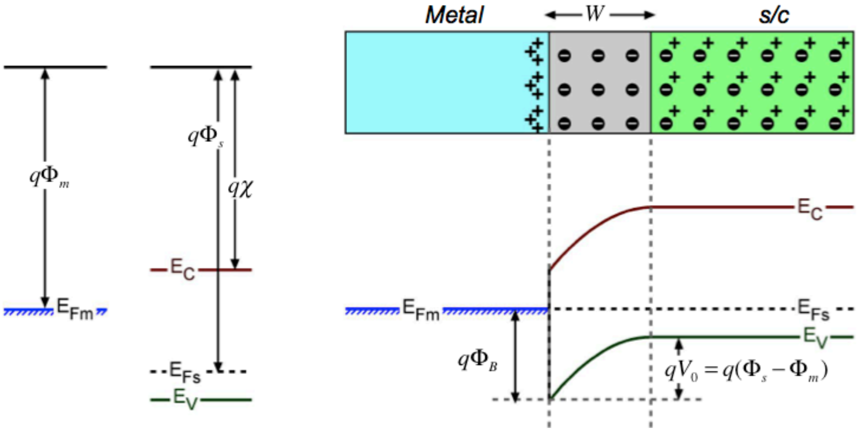






The middle two (they are rectifying). The outer two are ohmic and that would not work at all, no amplification!

(3) Now lets review the basics for a MESFET, which is a transistor where the input is a Schottky diode capacitor… Consider a metal-semiconductor (Schottky) diode with a p-type semiconductor.



(a) How would you calculate reverse bias capacitance for a metal-semiconductor (Schottky) diode with a p-type semiconductor? Give the revised formula as a function of the contact potential for the metal-semiconductor diode. For once, lets have YOU derive the formula on your own from something we already know…

$$W = \sqrt{\frac{2\varepsilon kT}{q^2}\left(\ln\frac{N_A N_D}{n_i^2}\right)\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$

Hint: above is depletion width for a PN junction. This is easy:

1. *replace the part of W above that is contact potential, with just Vo*
2. *then simplify further considering the metal is like n+++ and the p is therefore the lightly doped side*
3. *the use the simple parrelell plate capacitor formula to get capacitance!*

Note, kT/q out front (units of Volts!) and the ln function, which together is the formula for contact potential:

$$V_0 = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2}$$

So, all we need to do is substitute the contact potential in for the Schottky, and assume the metal is like n++, which gives us:

$W = \sqrt{\dfrac{2\varepsilon V}{qN_A}}$ where V is the metal work function minus the semiconductor workfunction minus any applied voltage (if any).

Notice also how is dependent on Na, if Na increases, we don't have to go as far to uncover the amount of charge we need to create the voltage!

$$C = \varepsilon A/W$$

$$C = \varepsilon A\left(\frac{2\varepsilon V}{qN_A}\right)^{-1/2} = \varepsilon A\left(\frac{qN_A}{2\varepsilon V}\right)^{1/2} = A\left(\frac{q\varepsilon N_A}{2V}\right)^{1/2}$$

(b) Well, once you have this formula from (a), you could calculate the capacitance per unit area, if you just knew the contact potential and the doping level… so lets do it!

The electron affinity for most semiconductors like Ge, Si, and GaAs is ~ 4.0 eV. Assume W metal with a workfunction of 4.6 eV is deposited onto Si doped to 10^{18} with Boron. <u>Calculate the contact potential</u>. *Hint: Remember, this doping shifts the Fermi level down (and therefore the semiconductor workfunction), by* $kT \times \ln(N_A/n_i)$. *So 1st, calculate the* *semiconductor workfunction. Just looking at the diagram, the work function (Phi) should be the electron affinity (Chi), plus ½ the bandgap, plus the amount the Fermi level shifted down from the undoped Fermi level.*

Phi(s)= Chi +Eg/2 + kT*ln(Na/ni) = 4 eV + 0.55 eV + 0.47 eV = 5.02 eV

Contact potential is therefore = 5.02 V – 4.6 V = 0.42 V

$$C/A = \left(\frac{q\varepsilon N_A}{2V}\right)^{1/2}$$ = 4.46E-7F/cm2 or 446 nF/cm2

(c) Last question, one thing we like about MESFETs is we can make small gates and therefore also small (short) channel lengths, for a given MESFET, if we decrease the gate by a factor of 5, how much will the RC time constant be reduced for each one of a bunch of MESFETs connected in a circuit? This shows you one reason why we like to make SMALLER transistors!

Hint, like in lecture, feed one MESFET into another, and the capacitance is due to the gates (the gate area) and the resistance is the previous MESFETs channel resistance (length).

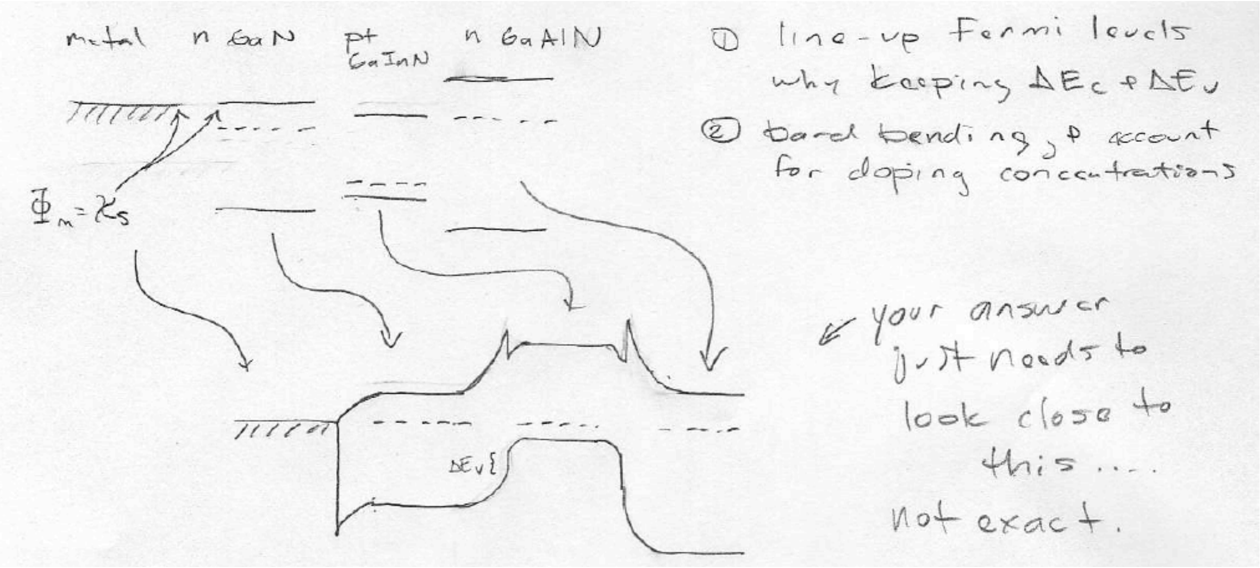
R goes down by 5 (channel length decreases by 5) and C goes down by 5 (gate area decreases by 5) for a RC time constant improvement of 25X! A very nice bang for your buck!

Further Problems (if you have time, finish during class when I can help, or on your own time)

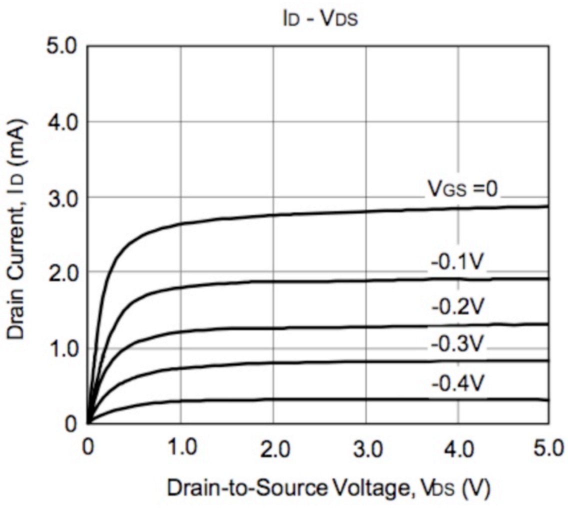
(4) This question is related to heterojunctions. The goal is to convince you that you know enough to create the band diagram for ANY set of semiconductors and metals. These are GaN semiconductors where the column III element (Ga) is partially replaced with other column III elements (such as In, and Al) to change the bandgap.

GaN has a bandgap of 3.4. GaAlN has a bandgap of 3.8 (only a little bit of Al added). GaInN has a bandgap of 3.1 (only a little bit of In added). You may assume that the Fermi levels for intrinsic versions of these materials would be equal.

Draw a band-diagram for a metal / n GaN / p+ GaInN / n GaAlN. Assume the metal workfunction is the same as the electron affinity for the GaN (which is the vacuum level to conduction band). The diagram need not be exact, but should be representative.



(5) Consider the transistor characteristics shown at right for a commercial JFET



a) The current saturates as Vds increases because:

___ the source-drain resistance kicks in.
_X_ the gate/drain pn junction grows and depletes the channel.
___ the gate/drain pn junction becomes forward biased.

b) The conducting channel for the source and drain is:

___ p-type.
_X_ n-type.
___ you can't tell, it could be either.

c) If we place this JFET in a circuit that has a 2 V drain voltage and an output resistance (JFET + external wires) of 0.5 kΩ, from your best estimate, what would be the value for I_D if V_{GS}= -0.25V? *Hint, draw a line on the plot above…*

You would draw a straight line from the 4.0 (2V/0.5kohm) on the y axis and 2.0 on the x-axis. Looking at where that intersects between the -0.2 and -0.3 V_{GS} curve, it would be I_D of about 1 mA.

d) Calculate the transconductance at saturation.

g_m ~$4x10^{-3}$ mhos

$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G} = \frac{(1.8-0.3)mA}{0.3\,V}$$